AMENDMENTS TO THE CLAIMS

1. (Original) A microcomputer including a plurality of peripheral circuits, comprising a connecting circuit that permits interconnection among the plurality of peripheral circuits to be controlled through execution of a program.

2. (Original) A microcomputer as claimed in claim 1, wherein the connecting circuit comprises a selector that selects one among a plurality of inputs and then outputs the selected input according to data given by the program.

3. (Original) A microcomputer as claimed in claim 1, wherein a circuit for writing data input to the peripheral circuits through execution of the program is provided as one of the peripheral circuits.

4. (Original) A microcomputer as claimed in claim 1, wherein a circuit for reading data output from the peripheral circuits through execution of the program is provided as one of the peripheral circuits.

5. (Original) A microcomputer as claimed in claim 1, wherein a circuit for inputting a signal from outside to the microcomputer is provided as one of the peripheral circuits.

6. (Original) A microcomputer as claimed in claim 1, wherein a circuit for outputting a signal generated inside the microcomputer to outside is provided as one of the peripheral circuits.

7. (Original) A microcomputer as claimed in claim 1, further comprising means for realizing a predetermined peripheral circuit function by controlling through the connecting circuit the interconnection among the plurality of peripheral circuits.

8. (New) A microcomputer comprising:

a program for operating the microcomputer;

a plurality of peripheral circuits, each having an individual function and functioning interactively with each other; and

a connecting circuit connected to the peripheral circuits and comprising a plurality of selectors that select one from among a plurality of input signals and then output the selected input signal to the peripheral circuits according to data given by the program,

wherein the plurality of peripheral circuits includes an output register that, according to commands included in the program, latches and stores the data temporarily, and thereafter outputs the data to the connecting circuit;

a predetermined selector is selected by the program and the data is fed from the output register to the selected selector so that a signal to be outputted to the peripheral circuits is selected from among the plurality of input signals; and

thereby, interconnection among the plurality of peripheral circuits is changed.

9. (New) A microcomputer as claimed in claim 8,

wherein the plurality of peripheral circuits includes an input register that, according to the commands included in the program, latches and stores temporarily the data to be outputted from the peripheral circuits and thereafter outputs the data so that the data is taken into the microcomputer.

10. (New) A microcomputer as claimed in claim 8,

wherein the plurality of peripheral circuits includes a logic circuit for inputting an external signal to the peripheral circuits.

11. (New) A microcomputer as claimed in claim 8,

wherein the plurality of peripheral circuits includes a logic circuit for outputting externally a signal generated within the peripheral circuits.

12. (New) A microcomputer as claimed in claim 10,

wherein the peripheral circuits to which the external signal is inputted is a timer for measuring periods for which the external signal remains at a high level and a low level respectively.

13. (New) A microcomputer as claimed in claim 10,

wherein the peripheral circuits to which the external signal is inputted include a first timer that starts counting on a trailing edge of the external signal and stops counting on a rising edge thereof subsequent to the trailing edge and a second timer that starts counting on a rising edge of the external signal and stops counting on a trailing edge thereof subsequent to the rising edge.

14. (New) A microcomputer as claimed in claim 11,

wherein the plurality of peripheral circuits for generating the signal to be outputted externally includes a first timer and a second timer and generates a signal having a high level for a

predetermined period and a low level for another predetermined period by changing said interconnection by way of the connecting circuit.